SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation Application of PCT Application No. PCT/JP2014/051967, filed Jan. 29, 2014 and based upon and claiming the benefit of priority from Japanese Patent Application No. 2013-096286, filed May 1, 2013, the entire contents of all of which are incorporated herein by reference.

FIELD

A present embodiment relates to a semiconductor device including a metal Ge compound layer on a semiconductor layer including Ge as a main component, and also relates to a method for manufacturing the semiconductor device.

BACKGROUND

With regard to a Ge-MOSFET which is expected to be a next-generation device, application of a germanide, such as NiGe, to a metal contact to a source/drain (S/D) or metal S/D has been studied. The germanide is advantageous in that an S/D resistance is lower than that in n^+-Ge or p^+-Ge formed by high-concentration doping of an impurity and that the germanide can be formed on a Ge layer in a self-aligning manner.

However, in a case of forming a germanide by deposition of a metal on a Ge layer and annealing of the metal and Ge, the germanide is polycrystalline and disadvantageous in that an interface has a low degree of flatness. In the case of Ge nMOSFET with metal S/D, a contact resistance between the germanide S/D and an n-type (or p-type) Ge is increased (or reduced), accordingly, an on (off) current is reduced (or increased).

The reason for this may be that a Fermi level of a germanide is pinned to a charge neutral level near a valence band of Ge (Fermi level pinning: FLP). With increasing of the interface states, the FLP becomes stronger. Therefore, an interface having a high degree of flatness is desirable to lower interface state.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagram showing a TEM image of NiGe epitaxially grown on a Ge(100) plane and positions of TEM-EDX measurement.

FIG. **2** is an enlarged view of a TEM image of an interface portion between NiGe and Ge shown in FIG. **1**.

FIG. **3** is a diagram showing a relationship between energy and X-ray intensity analyzed by TEM-EDX.

FIG. **4** is a diagram showing a spot pattern by FFT of the TEM image shown in FIG. **1**.

FIG. **5** is a diagram showing a TEM image in which lattices of NiGe and lattices of Ge(100) are formed such that the respective lattice spacings match.

FIG. **6** is a diagram showing current-voltage characteristics of NiGe/nGe.

FIG. **7** is a schematic diagram showing a relationship between an extraction direction and an extraction width in an EDX analysis.

FIG. **8** is a diagram showing a composition distribution by an EDX analysis.

FIG. **9** is a diagram showing a TEM image in a case of forming an NiGe layer on a Ge layer (Ni: 10 nm, Sn: 1 nm).

FIG. **10** is a diagram showing a TEM image in a case of forming an NiGe layer on a Ge layer (Ni: 5 nm, Sn: 1 nm).

FIG. **11** is a diagram showing a TEM image in a case of forming an NiGe layer without Sn (Ni: 10 nm).

FIG. **12** is a diagram showing a TEM image of an NiGe layer before HCl treatment.

FIG. **13** is a diagram showing composition distributions at analysis points in the NiGe layer shown in FIG. **12**.

FIG. **14** is a cross-sectional view of a schematic configuration of an NiGe-S/D-Ge-nMOSFET according to the present embodiment.

FIG. **15** is a cross-sectional view showing a process of manufacturing the nMOSFET shown in FIG. **14**.

DETAILED DESCRIPTION

In general, according to one embodiment, the semiconductor device includes a semiconductor layer including Ge; and a metal Ge compound region provided in a surface portion of the semiconductor layer, wherein Sn is included in an interface portion between the semiconductor layer and the metal Ge compound region, and a lattice plane of the semiconductor layer matches with a lattice plane of the metal Ge compound region.

Embodiment

Outline

An outline of the present embodiment will be explained, before examples of the present embodiment are explained.

As described above, in a case of forming a compound layer, such as an NiGe layer, on a Ge layer, the NiGe layer is polycrystalline and an interface having low flatness is formed between the Ge layer and the NiGe layer.

The present inventors have studied various methods for growing a single crystal of NiGe at an interface having a high degree of flatness on a Ge layer. As a result, the present inventors conceived a structure including an Sn layer inserted in an interface between Ni and Ge, and discovered that when the structure is subjected to annealing (heat treatment), an NiGe layer having a high degree of interface flatness in a wide range can be epitaxially grown on a Ge layer, as shown in a TEM image (in a cross section) of FIG. **1** and an enlarged view of FIG. **2**. For example, when an Ni (10 nm)/Sn (1-5 nm)/Ge(100) structure is subjected to annealing (350° C., 1 min.), a single crystal of NiGe (14 nm) having a high degree of interface flatness is formed. The size of the single-crystal NiGe ranges as wide as 100 nm to 500 nm.

It was verified, by TEM-EDX (energy dispersive X-ray spectrometry), that the composition ratio of Ni to Ge in the NiGe thus formed was nearly 1:1. For example, FIG. **3** shows a result of an analysis of a composition at point 3 in the TEM image of FIG. **1** (in a cross section). In FIG. **3**, a horizontal axis represents energy, and a vertical axis represents an X-ray intensity. At point 3 in the crystal, the contents of Ni and Ge are respectively 53.92 at. % and 45.7 at. %; thus, the ratio thereof is nearly 1. The content of Sn in the crystal is 0.38 at. %, which is negligible.

It was also verified from the TEM image, by fast Fourie transform (FFT), that the NiGe structure formed by the above method was orthorhombic as well as a conventionally formed NiGe structure. Lattice spacings and an angle